100 N-channel Power MOSFET

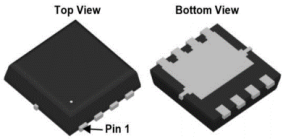
DESCRIPTION：

- Low On-Resistance
- Excellent FoM (figure of merit)
- 100% ΔVDS & UIS & Rg Tested
- Halogen-free；RoHS-compliant
- Pb-free plating

V_{DS}	100V
I_{D_MAX}	32A
$R_{DS(ON)_typ}$ @V_{GS}=10V	13.6mΩ

TYPICAL APPLICATIONS：

- Motor controls
- DC/DC in Telecoms and Industrial
- High frequency switching, synchronous rectification



PDFN3×3-8L

MAXIMUM RATINGS (at T_C = 25 °C, unless otherwise specified)

Characteristic	Condition	Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (1)	Tc=25℃ Tc=100℃	I_D	32 20	A
Pulsed Drain Current (2)		I_{DM}	129	A
Single Pulsed Avalanche Energy (3)		E_{AS}	90	mJ
Power dissipation	Tc=25℃ Tc=100℃	P_D	32 13	W
Junction & Storage temperature Range		T_J, T_{STG}	-55~+150	℃

Notes： 1. This current is chip limited, which is calculated based on Rthjc.
2. This current is calculated on single pulse with 10us Single Pulse.
3. Defined by design, not subject to production test, EAS condition: TJ=25°C, VDD=50V, VGS=10V, L=1.0mH.

THERMAL CHARACTERISTICS

Characteristic	Condition	Symbol	Value	Unit
Thermal resistance,	Junction to Ambient Junction to Case	$R_{\theta JA}$ $R_{\theta JC}$	52 3.0	℃/W

ELECTRICAL CHARATERISTICS (at T_J = 25 °C, unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage VGS = 0V, ID = 250uA	$V_{(BR)DSS}$	100			V
Zero Gate Voltage Drain Current VDS = 100V, VGS = 0 V	I_{DSS}			1.0	uA
Gate-Source Leakage Current VGS = ±20V, VDS = 0V	I_{GSS}			±100	nA
Gate-Source threshold voltage VDS = VGS, ID = 250uA	$V_{GS(th)}$	1.2	1.7	2.5	V
Drain-Source On-State Resistance VGS = 10V, ID = 15A VGS = 4.5V, ID =10A	$R_{DS(on)}$		13.6 15.9	16.3 20	mΩ
Gate Resistance f=1MHz	Rg		1.2		Ω
Input capacitance f=1MHz, VDS=50V, VGS=0 V	C_{iss}		745		pF
Output capacitance f=1MHz, VDS=50V, VGS=0 V	C_{oss}		331		pF
Reverse transfer capacitance f=1MHz, VDS=50V, VGS=0 V	C_{rss}		8.5		pF
Total Gate Charge VDS= 50V, ID= 15A,VGS= 10V	Q_G		13.0		nC
Gate to Source Charge VDS= 50V, ID= 15A,VGS= 10V	Q_{GS}		2.2		nC
Gate to Drain Charge VDS= 50V, ID= 15A,VGS= 10V	Q_{GD}		2.8		nC
Turn-on delay time VDS=50 V, VGS= 10V, ID=15A, R_{GEN}=3Ω	td (ON)		2.9		ns
Rise time VDS=50 V, VGS= 10V, ID=15A, RGEN=3Ω	tr		3.0		ns
Turn-off delay time VDS=50 V, VGS= 10V, ID=15A, RGEN=3Ω	td (OFF)		12.2		ns
Fall time VDS=50 V, VGS= 10V, ID=15A, RGEN=3Ω	tf		4.9		ns
Maximum Continuous Body Diode Forward Current	IS			32	A
Diode Forward Voltage VGS = 0V, I_S =2.0A	V_{SD}			1.2	V
Revers Recovery Time IF=15A, di/dt = 100A/us	Trr		44		ns
Revers Recovery Charge IF=15A, di/dt = 100A/us	Qrr		27		nC

Typical Performance Characteristics

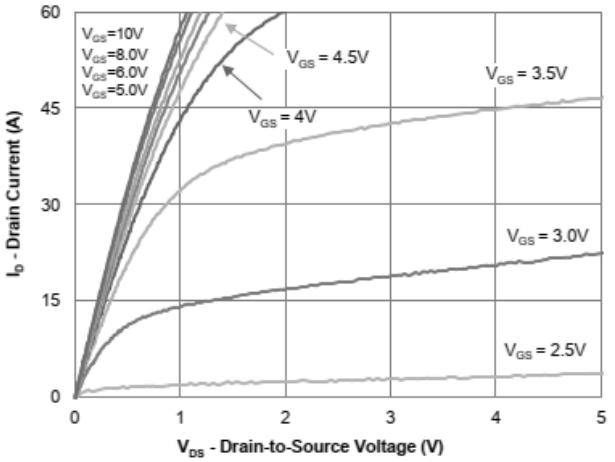


Figure 1: Output Characteristics

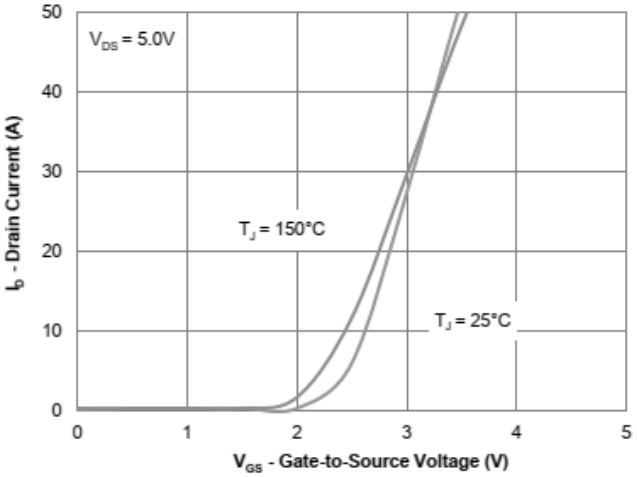


Figure 2. Transfer Characteristics

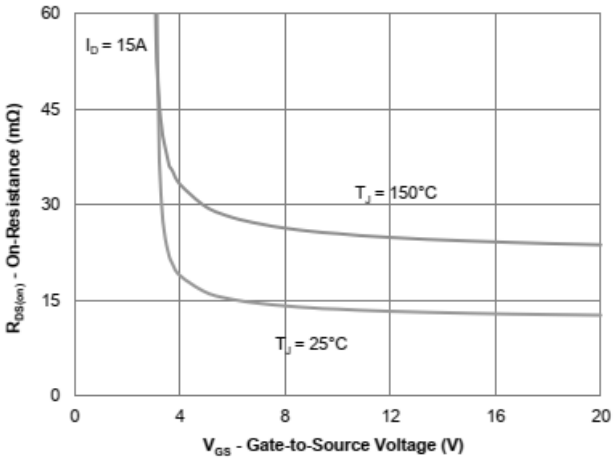


Figure 3. On-Resistance vs. Gate-Source Voltage

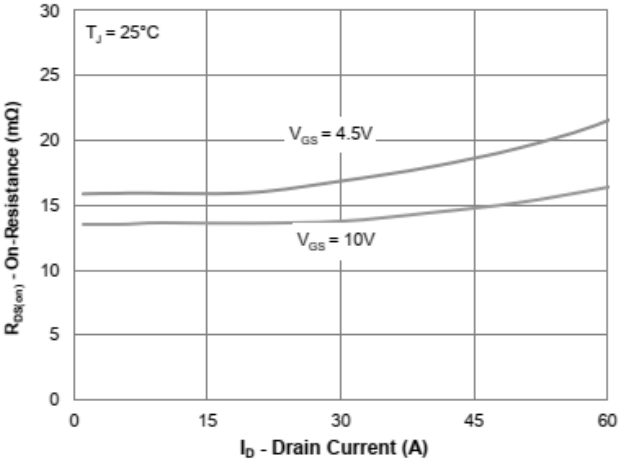


Figure4. On-Resistance vs. Drain Current and Gate Voltage

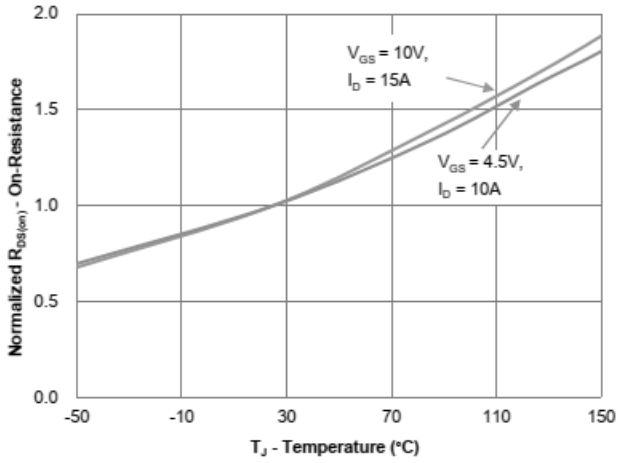


Figure 5. On-Resistance vs. Gate-Source Volt

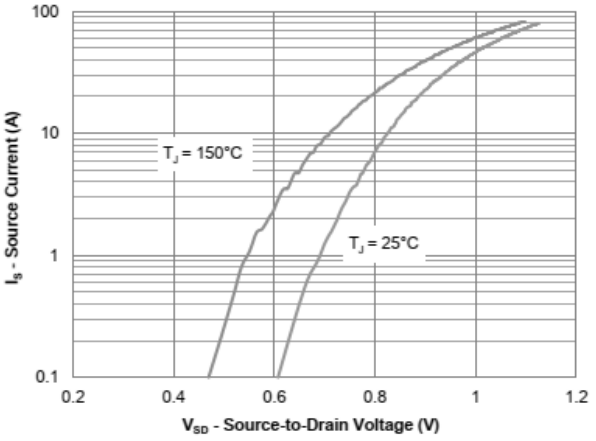


Figure 6. Source-Drain Diode Forward Voltage

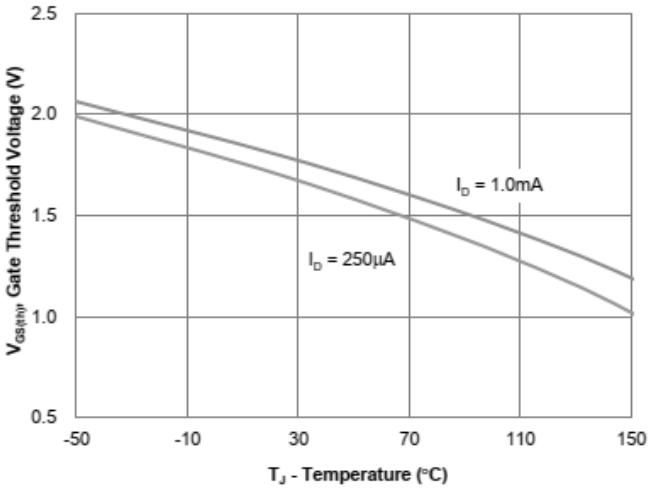


Figure 7. Gate Threshold Variation vs. Junction Temperature

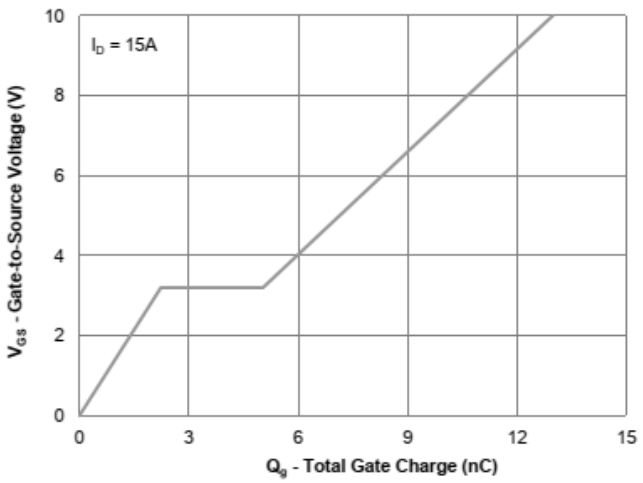


Figure 8. Gate Charge Characteristics

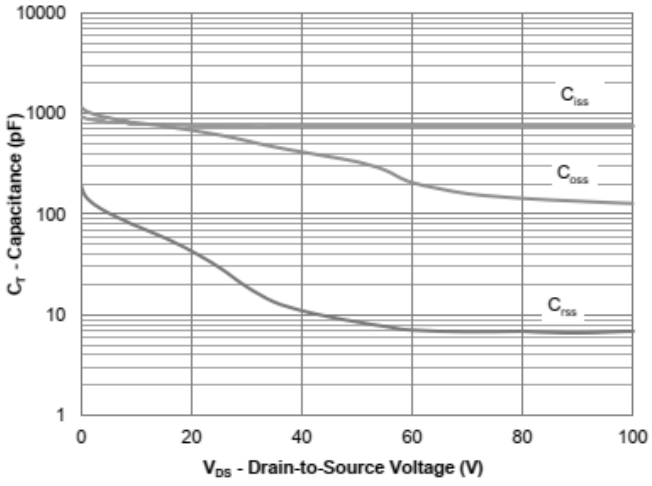


Figure 9. Capacitance Characteristics

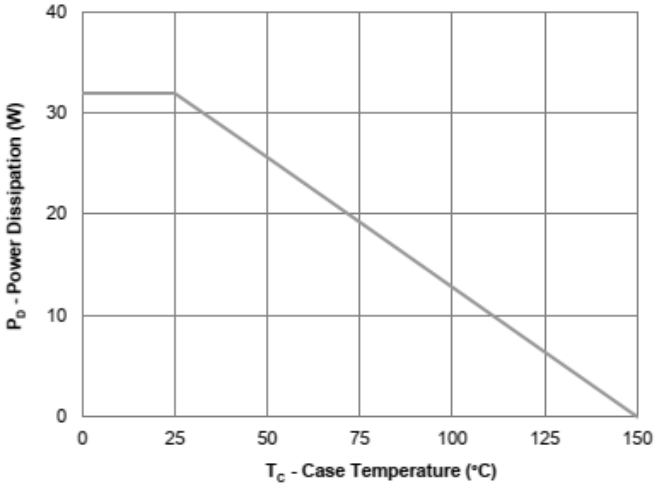


Figure 10. Power Derating

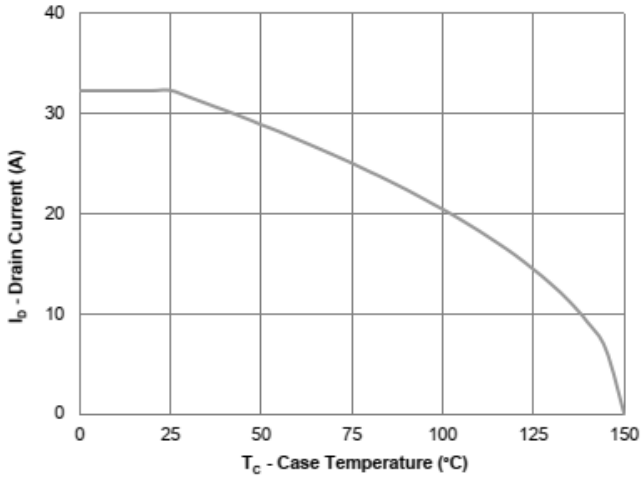


Figure 11. Current Derating

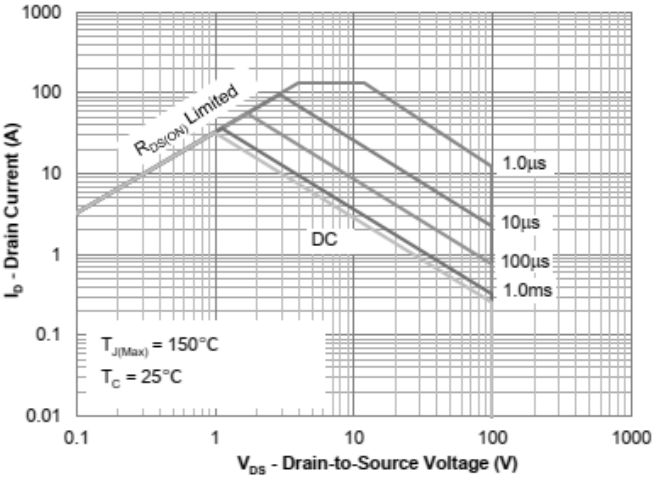
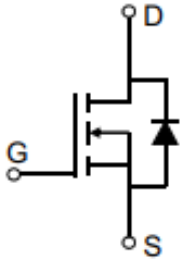
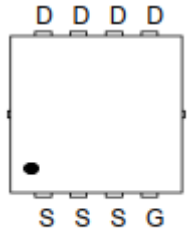


Figure 12. Safe Operating Area

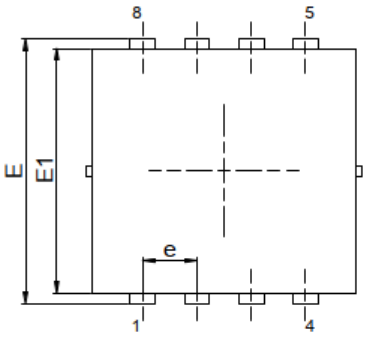
• Circuit diagram



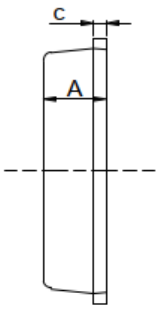


PIN Configuration
(Top View)

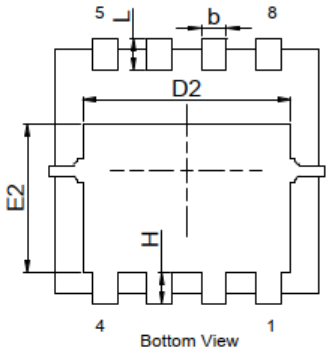
• Package outlines : Dimensions in (mm)



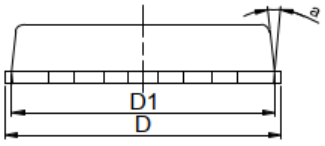
Top View



Side View



Bottom View



Front View

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.80	0.90
b	0.20	0.30	0.40
c	0.10	0.15	0.25
D	3.10	3.30	3.40
D1	3.00	3.15	3.25
D2	2.35	--	2.69
E	3.20	3.35	3.45
E1	2.85	3.10	3.20
E2	1.48	--	1.98
e	0.65 BSC		
H	0.25	--	0.60
L	0.25	0.40	0.50
a	---	---	15°

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