100V N-Channel Power MOSFET

DESCRIPTION：

- Excellent $R_{DS(ON)}$
- Low Gate Charge
- 100% UIS Tested, 100% △Vds Tested
- Pb-Free Lead Plating
- RoHS compliant
- Halogen Free

V_{DS}	100V
I_D (Tc=25℃)	120A
$R_{DS(ON)\_Typ.}$ @V_{GS}=10V	11.6mΩ

TYPICAL APPLICATIONS：

- Power Management
- Load Switch
- PWM Application

TO-247-3L

MAXIMUM RATINGS (at T_C = 25 °C, unless otherwise specified)

Characteristic	Condition	Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current		I_D	120	A
Single Pulsed Avalanche Energy (1)		E_{AS}	144	mJ
Junction & Storage temperature Range		T_J, T_{STG}	-55~+150	℃

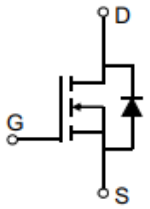
Notes： 1. EAS condition: Starting TJ=25℃, VDD=50V, VGS=10V, RG=25ohm, L=0.5mH, IAS=24A, VDD=0V during time in avalanche.

ELECTRICAL CHARATERISTICS (at T_J = 25 °C, unless otherwise specified)

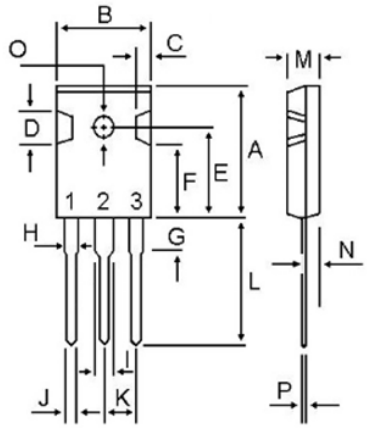
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage VGS = 0V, ID = 250uA	$V_{(BR)DSS}$	100			V
Zero Gate Voltage Drain Current VDS = 100 V, VGS = 0 V	I_{DSS}			1	uA
Gate-Source Leakage Current VGS = ±20V, VDS = 0V	I_{GSS}			±100	nA

Gate-Source threshold voltage VDS = VGS, ID = 250uA	$V_{GS(th)}$	2.0	3.0	4.0	V
Drain-Source On-State Resistance VGS = 10V, ID = 30A VGS = 8V, ID = 30A	$R_{DS(on)}$		11.6 12.2	15.0 16.0	mΩ
Input capacitance f=1MHz, VDS=50 V, VGS=0 V	C_{iss}		4930		pF
Output capacitance f=1MHz, VDS=50 V, VGS=0 V	C_{oss}		180		pF
Reverse transfer capacitance f=1MHz, VDS=50 V, VGS=0 V	C_{rss}		168		pF
Gate Resistance f=1MHz, VDS=0 V, VGS=0 V	R_g		0.7		Ω

- Circuit diagram



- TO-247-3L Package outlines : Dimensions in (mm)



DIM	MILLIMETERS	
	MIN	MAX
A	20.80	21.80
B	15.38	16.20
C	1.90	2.70
D	5.10	6.10
E	14.50	15.50
F	11.20	13.20
G	3.75	4.35
H	1.90	2.30
I	2.90	3.30
J	1.00	1.40
K	5.26	5.66
L	19.50	20.50
M	4.68	5.36
N	2.30	2.60
O	3.45	3.85
P	0.48	0.72

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