MOSPEC

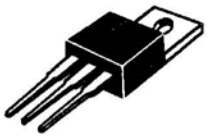
PNP SILICON POWER TRANSISTORS

D45H1A transistor is designed for use in low voltage and low drop-out regulator switching circuits application

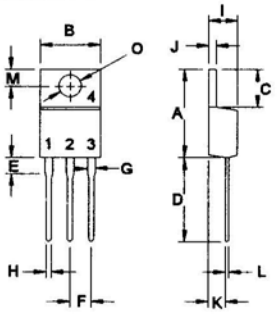
PNP
D45H1A

FEATURES:
* Collector-Emitter Voltage
  V_{CEO}= 15V(Min)
* High Current Power Transistors
* DC Current Gain
  hFE= 70 (Min.)@I_C= 8.0A

10 AMPERE
POWER
TRANASISTORS
15 VOLTS
60 WATTS



TO-220



PIN 1.BASE
2.COLLECTOR
3.EMITTER
4.COLLECTOR(CASE)

DIM	MILLIMETERS	
	MIN	MAX
A	14.68	16.00
B	9.78	10.42
C	5.02	6.60
D	13.00	14.62
E	3.10	4.19
F	2.41	2.67
G	1.10	1.67
H	0.69	1.01
I	3.21	4.98
J	1.14	1.40
K	2.20	3.30
L	0.28	0.61
M	2.48	3.00
O	3.50	4.00

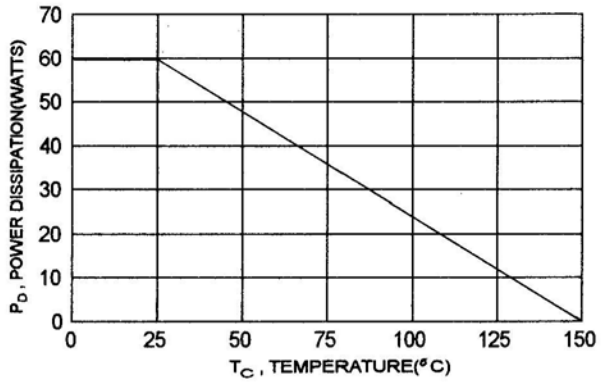
MAXIMUM RATINGS

Characteristic	Symbol	D45H1A	Unit
Collector-Emitter Voltage	V_{CEO}	15	V
Collector-Base Voltage	V_{CBO}	20	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Collector Current - Continuous - Peak	I_C I_{CM}	10 20	A
Total Power Dissipation @T_C = 25°C Derate above 25°C	P_D	60 0.48	W W/°C
Operating and Storage Junction Temperature Range	T_J , T_{STG}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	Rθjc	2.08	°C/W

FIGURE -1 POWER DERATING



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Voltage (I_C= 30 mA, I_B= 0)	V_{CEO}	15		V
Collector Cutoff Current (V_{CB}= 20 V, I_E= 0)	I_{CBO}		10	uA
Emitter Cutoff Current (V_{EB}= 5.0 V, I_C= 0)	I_{EBO}		10	uA
ON CHARACTERISTICS (1)				
DC Current Gain (I_C= 8.0 A, V_{CE}= 1.0 V)	hFE	70		
Collector-Emitter Saturation Voltage (I_C= 8.0 A, I_B= 400 mA)	$V_{CE(sat)}$		0.6	V
Base-Emitter Saturation Voltage (I_C= 8.0 A, I_B= 400 mA)	$V_{BE(sat)}$		1.5	V

(1) Pulse Test: Pulse Width =300μ s,Duty Cycle ≦ 2.0%:

FIG-2 DC CURRENT GAIN

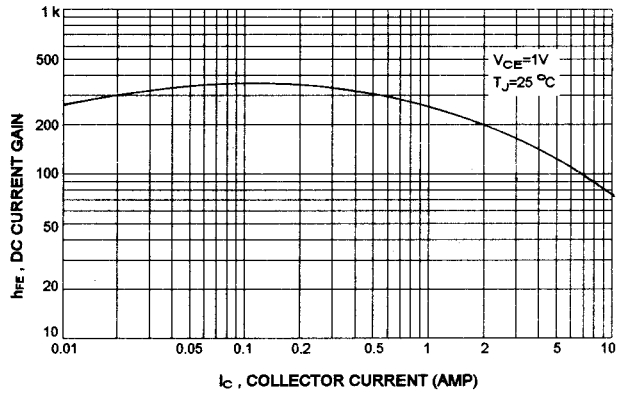


FIG-3 COLLECTOR SATURATION REGION

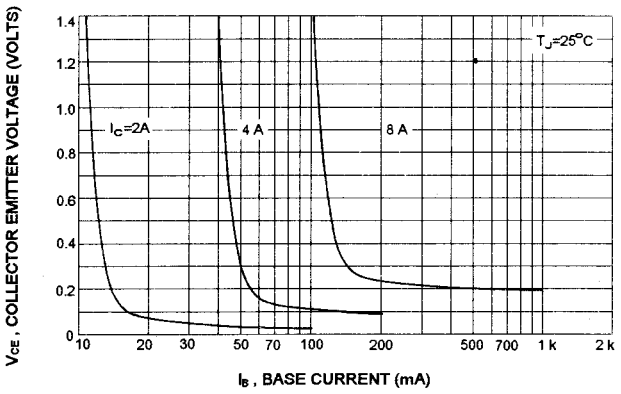
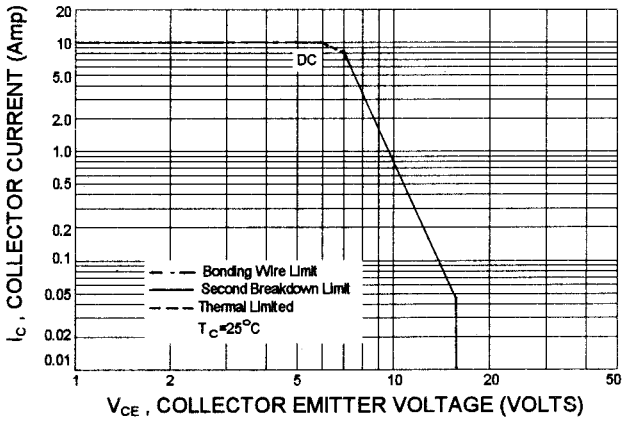


FIG-4 SAFE OPERATING AREA



There are two limitation on the power handling ability of a transistor:average junction temperature and second breakdown safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of FIG-4 is base on $T_{J(PK)}$=150 °C;T_C is variable depending on power level.second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(PK)}$ <150°C,At high case temperatures, thermal limitation will reduce the power that can be handled to Values less than the limitations imposed by second breakdown.

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