

HORIZONTAL DEFLECTION TRANSISTORS

...designed for use in large screen color deflection circuits

FEATURES:

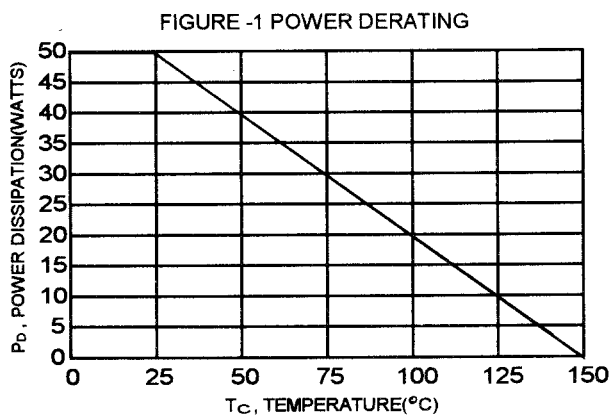
- * Collector-Emitter Sustaining Voltage
 $V_{CE(sus)} = 500V(\text{Min})$
- * Fast Switching Time
 $t_r = 1.0 \mu s @ I_C = 4.0A$
- * Glass Passivated Collector-Base Junction

MAXIMUM RATINGS

Characteristic	Symbol	2SC1358	Unit
Collector-Emitter Voltage	V_{CEO}	500	V
Collector-Base Voltage	V_{CBO}	1400	V
Emitter-Base Voltage	V_{EBO}	6.0	V
Collector Current - Continuous - Peak	I_C I_{CM}	4.5 10	A
Base current	I_B	1.5	A
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	50 0.4	W W/ $^\circ C$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-65 to +150	$^\circ C$

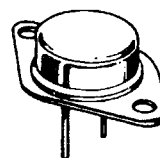
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	$R_{\theta jc}$	2.5	$^\circ C/W$

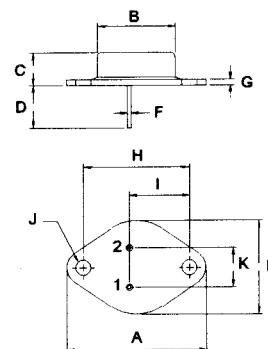


NPN
2SC1358

4.5 AMPERE
NPN SILICON
POWER TRANSISTORS
1400 VOLTS
50 WATTS



TO-3



PIN 1.BASE
2.EMITTER
COLLECTOR(CASE)

DIM	MILLIMETERS	
	MIN	MAX
A	38.75	39.96
B	19.28	22.23
C	7.96	9.28
D	11.18	12.19
E	25.20	26.67
F	0.92	1.09
G	1.38	1.62
H	29.90	30.40
I	16.64	17.30
J	3.88	4.36
K	10.67	11.18

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Voltage ($I_C = 100\text{ mA}$, $I_B = 0$)	V_{CE0}	500		V
Collector Cutoff Current ($V_{CE} = 1400\text{ V}$, $V_{BE} = 0$)	I_{CES}		1.0	mA
Collector Cutoff Current ($V_{CB} = 1000\text{ V}$, $I_E = 0$)	I_{CBO}		20	μA
Emitter Cutoff Current ($V_{EB} = 5.0\text{ V}$, $I_C = 0$)	I_{EBO}		200	μA

ON CHARACTERISTICS (1)

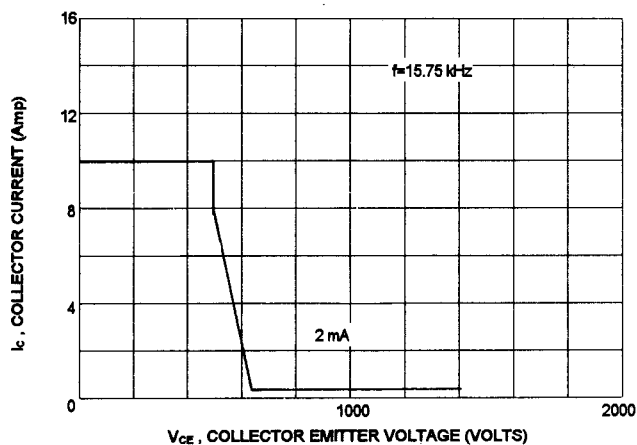
DC Current Gain ($I_C = 0.5\text{ A}$, $V_{CE} = 15\text{ V}$) ($I_C = 3.0\text{ A}$, $V_{CE} = 15\text{ V}$)	h_{FE}	10 5.0	45 35	
Collector-Emitter Saturation Voltage ($I_C = 4.0\text{ A}$, $I_B = 0.8\text{ A}$)	$V_{CE(sat)}$		10	V
Base-Emitter Saturation Voltage ($I_C = 4.0\text{ A}$, $I_B = 0.8\text{ A}$)	$V_{BE(sat)}$		1.2	V

SWITCHING CHARACTERISTICS

Storage Time	$I_C = 4.0\text{ A}$, $I_{B1} = -I_{B2} = 1.0\text{ A}$ $PW = 20\text{ }\mu\text{s}$	t_s	10	μs
Fall Time		t_f	1.0	μs

(1) Pulse Test: Pulse Width $\approx 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$

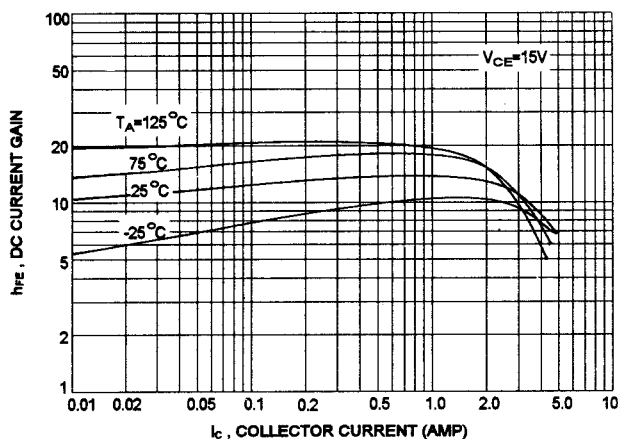
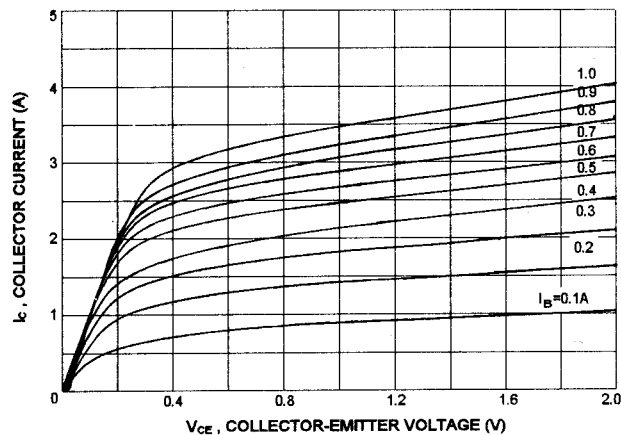
ACTIVE-REGION SAFE OPERATING AREA (SOA)



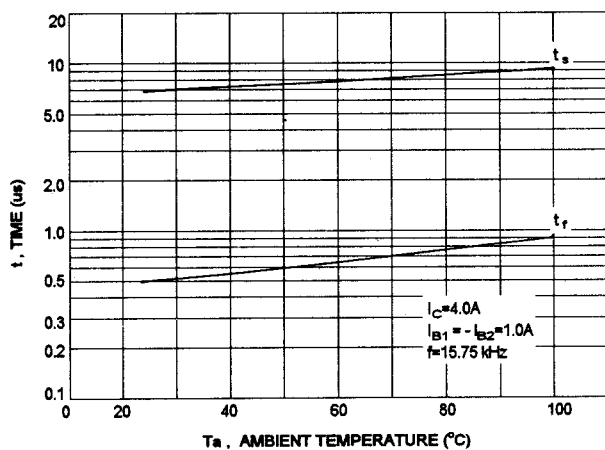
There are two limitation on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of SOA curve is base on $T_{J(PK)}=150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(PK)} \leq 150^\circ\text{C}$. At high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

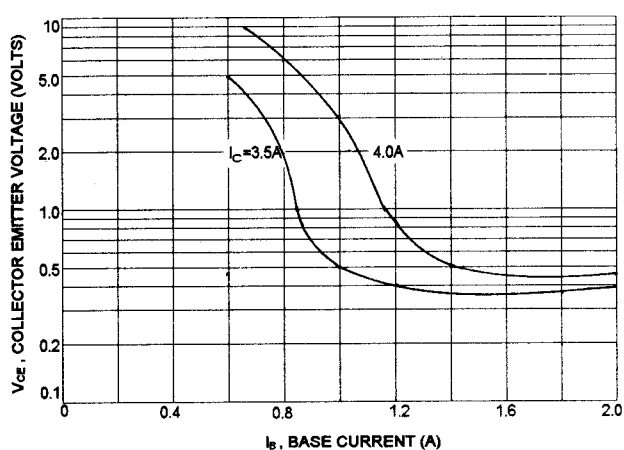
DC CURRENT GAIN

 I_C - V_{CE} 

SWITCHING TIME- AMBIENT TEMPERATURE



COLLECTOR SATURATION REGION



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