MOSPEC

PNP SILICON POWER TRANSISTORS

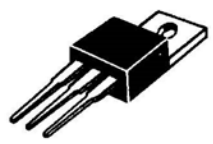
...designed for use in general power amplifier application

FEATURES:

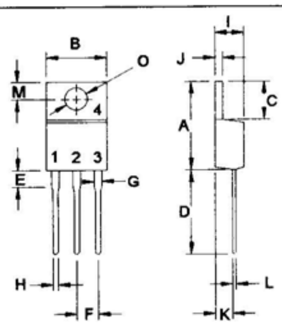
* Low Collector-Emitter Saturation Voltage
  $V_{CE(sat)}$= 1.0V(Max) @I_C=3.0A,I_B=0.3A
* DC Current Gain
  hFE= 40-240@I_C= 0.5A
* Complementary to NPN 2SD526

PNP
2SB596

4.0 AMPERE
POWER
TRANASISTORS
80 VOLTS
30 WATTS



TO-220



PIN 1.BASE
2.COLLECTOR
3.EMITTER
4.COLLECTOR(CASE)

DIM	MILLIMETERS	
	MIN	MAX
A	14.68	16.00
B	9.78	10.42
C	5.02	6.60
D	13.00	14.62
E	3.10	4.19
F	2.41	2.67
G	1.10	1.67
H	0.69	1.01
I	3.21	4.98
J	1.14	1.40
K	2.20	3.30
L	0.28	0.61
M	2.48	3.00
O	3.50	4.00

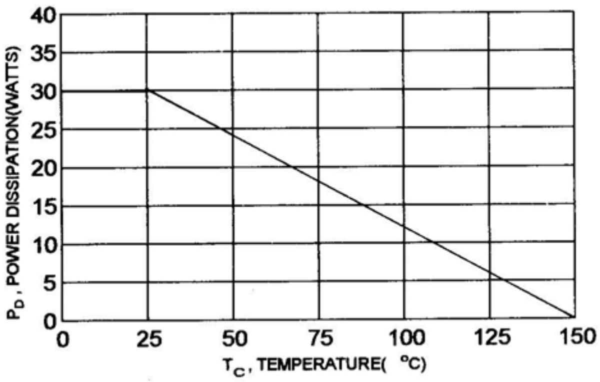
MAXIMUM RATINGS

Characteristic	Symbol	2SB596	Unit
Collector-Emitter Voltage	V_{CEO}	80	V
Collector-Base Voltage	V_{CBO}	80	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Collector Current - Continuous - Peak	I_C I_{CM}	4.0 8.0	A
Base current	I_B	2.0	A
Total Power Dissipation @T_C = 25°C Derate above 25°C	P_D	30 0.24	W W/°C
Operating and Storage Junction Temperature Range	T_J ,T_{STG}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	$R\theta jc$	4.16	°C/W

FIGURE -1 POWER DERATING



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

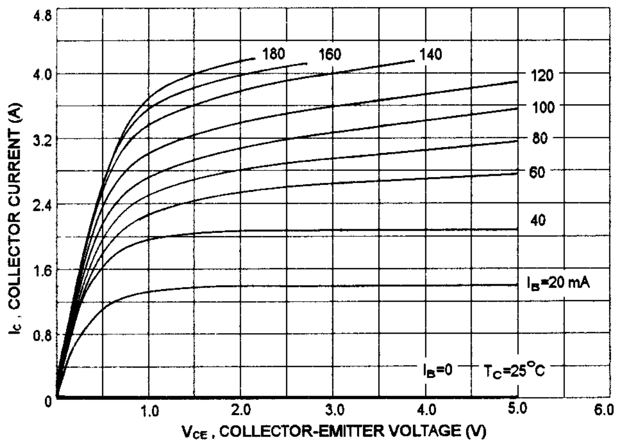
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C= 50 mA, I_B= 0)	$V_{(BR)CEO}$	80		V
Emitter-Base Breakdown Voltage (I_C= 10 mA, I_C= 0)	$V_{(BR)EBO}$	5.0		V
Collector Cutoff Current (V_{CB}= 80 V, I_E= 0)	I_{CBO}		30	uA
Emitter Cutoff Current (V_{EB}=5.0 V, I_C= 0)	I_{EBO}		100	uA
ON CHARACTERISTICS (1)				
DC Current Gain (I_C= 0.5 A, V_{CE}= 5.0 V) * (I_C= 3.0 A, V_{CE}= 5.0 V)	 hFE(2) hFE	 40 15	 240	
Collector-Emitter Saturation Voltage (I_C= 3.0 A, I_B= 300 mA)	$V_{CE(sat)}$		1.7	V
Base-Emitter On Voltage (I_C= 3.0 A, V_{CE}=5.0 V)	$V_{BE(on)}$		1.5	V
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 0.5 A, V_{CE} = 5.0 V, f = 1.0 MHz)	f_T	3.0		MHz

(1) Pulse Test: Pulse Width =300 us,Duty Cycle ≦ 2.0%

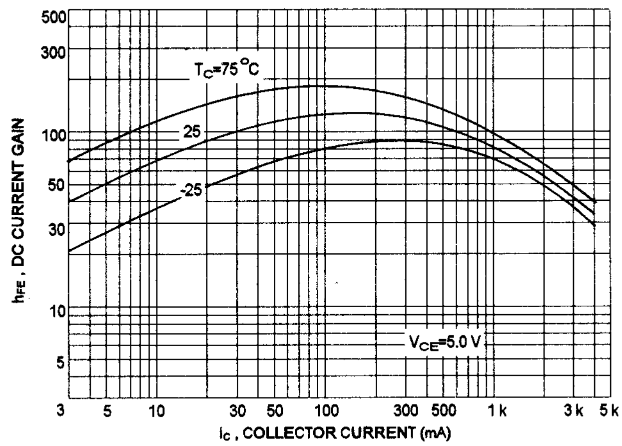
* hFE(2) Classification :

40- R 80	70 O 140	120 Y 240

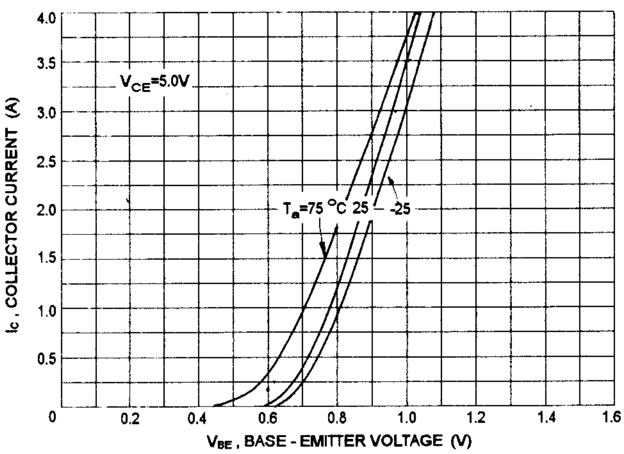
Ic - Vce



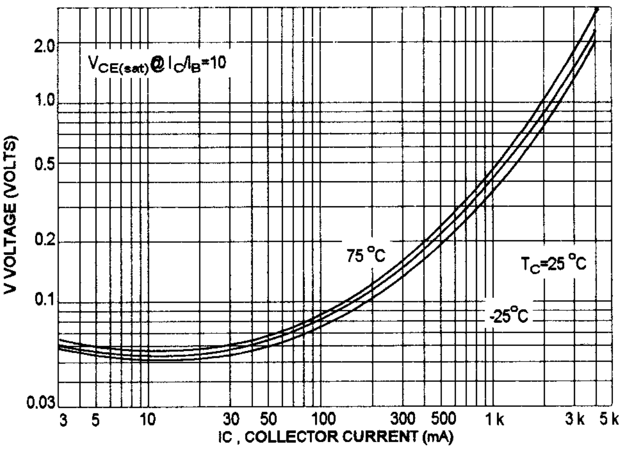
DC CURRENT GAIN



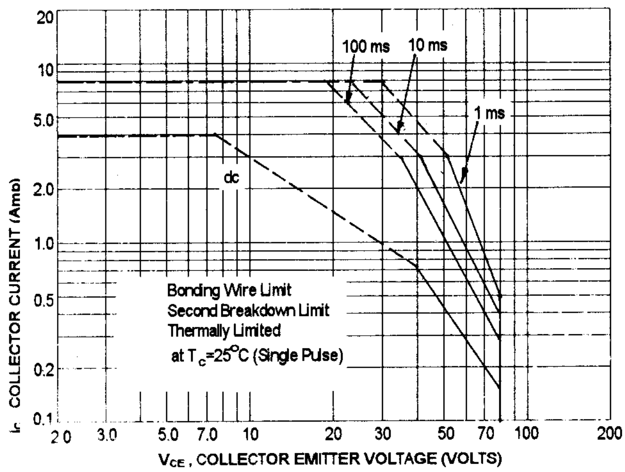
Ic - Vbe



$V_{CE(sat)}$-I_C



ACTIVE-REGION SAFE OPERATING AREA (SOA)



There are two limitation on the power handling ability of a transistor:average junction temperature and second breakdown safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of SOA curve is base on $T_{J(PK)}$=150 °C;T_C is variable depending on conditions. second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(PK)} \leq 150$°C,At high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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