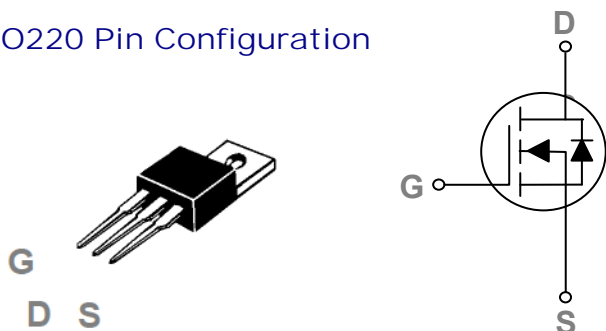


General Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

TO220 Pin Configuration



BVDSS	RDS(ON)	ID
40V	2.5mΩ	160A

Features

- 40V, 160A, $R_{DS(ON)} = 2.5m\Omega @ V_{GS} = 10V$
- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Green Device Available

Applications

- MB / VGA / Server Vcore
- POL Applications
- SMPS 2nd SR
- BMS System

Absolute Maximum Ratings $T_c=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous ($T_c=25^\circ\text{C}$) (Chip Limitation)	160	A
	Drain Current – Continuous ($T_c=100^\circ\text{C}$) (Chip Limitation)	100	A
I_{DM}	Drain Current – Pulsed ¹	640	A
EAS	Single Pulse Avalanche Energy ²	360	mJ
IAS	Single Pulse Avalanche Current ²	85	A
P_D	Power Dissipation ($T_c=25^\circ\text{C}$)	184	W
	Power Dissipation – Derate above 25°C	1.47	W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction to ambient	---	62	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction to Case	---	0.68	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Static State Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	40	---	---	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=40V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=32V$, $V_{GS}=0V$, $T_J=85^\circ\text{C}$	---	---	10	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
$R_{DS(ON)}$	Static Drain-Source On-Resistance ³	$V_{GS}=10V$, $I_D=30A$	---	2.1	2.5	$m\Omega$
		$V_{GS}=4.5V$, $I_D=15A$	---	2.6	3.5	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1	1.6	2.5	V
gfs	Forward Transconductance	$V_{DS}=10V$, $I_D=15A$	---	45	---	S

Dynamic Characteristics

Q_g	Total Gate Charge ^{3, 4}	$V_{DS}=20V$, $V_{GS}=4.5V$, $I_D=10A$	---	70	140	nC
Q_{gs}	Gate-Source Charge ^{3, 4}		---	15	32	
Q_{gd}	Gate-Drain Charge ^{3, 4}		---	40	80	
$T_{d(on)}$	Turn-On Delay Time ^{3, 4}	$V_{DD}=20V$, $V_{GS}=10V$, $R_G=10\Omega$ $I_D=10A$	---	24.6	48	ns
T_r	Rise Time ^{3, 4}		---	62.8	120	
$T_{d(off)}$	Turn-Off Delay Time ^{3, 4}		---	224	440	
T_f	Fall Time ^{3, 4}		---	162	320	
C_{iss}	Input Capacitance	$V_{DS}=25V$, $V_{GS}=0V$, $F=1\text{MHz}$	---	8000	12000	pF
C_{oss}	Output Capacitance		---	550	1000	
C_{rss}	Reverse Transfer Capacitance		---	420	800	
R_g	Gate resistance	$V_{GS}=0V$, $V_{DS}=0V$, $F=1\text{MHz}$	---	1.2	2.4	Ω

Guaranteed Avalanche Energy

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy	$V_{DD}=25V$, $L=0.1\text{mH}$, $I_{AS}=30A$	45	---	---	mJ

Drain-Source Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current	$V_G=V_D=0V$, Force Current	---	---	160	A
I_{SM}	Pulsed Source Current ³		---	---	320	A
V_{SD}	Diode Forward Voltage ³	$V_{GS}=0V$, $I_S=1A$, $T_J=25^\circ\text{C}$	---	---	1	V
t_{rr}	Reverse Recovery Time	$V_{GS}=0V$, $I_S=20A$, $di/dt=100A/\mu s$ $T_J=25^\circ\text{C}$	---	32	---	ns
Q_{rr}	Reverse Recovery Charge		---	19	---	nC

Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. $V_{DD}=25V$, $V_{GS}=10V$, $L=0.1\text{mH}$, $I_{AS}=85A$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$.
3. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
4. Essentially independent of operating temperature.

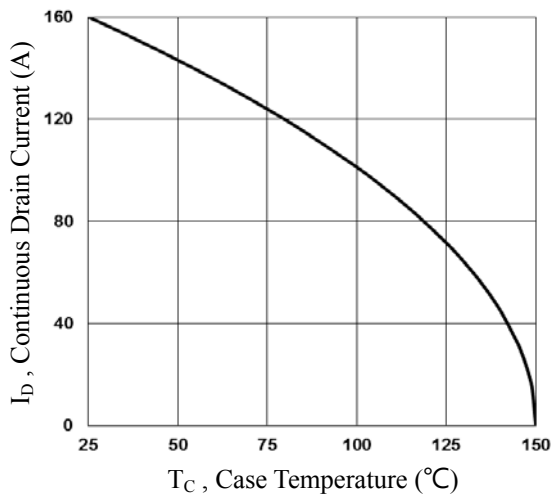


Fig.1 Continuous Drain Current vs. T_C

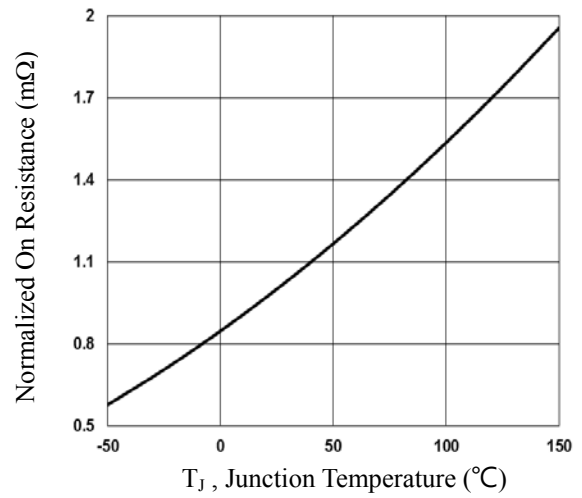


Fig.2 Normalized $R_{DS(on)}$ vs. T_J

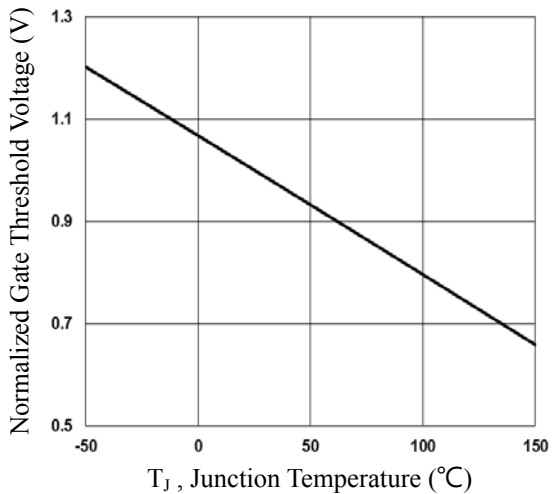


Fig.3 Normalized V_{th} vs. T_J

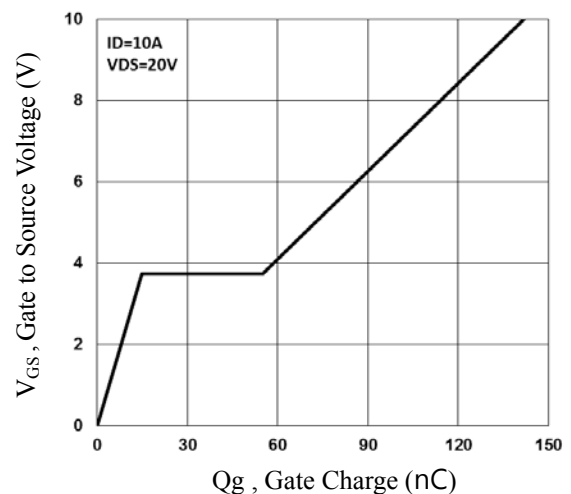


Fig.4 Gate Charge Waveform

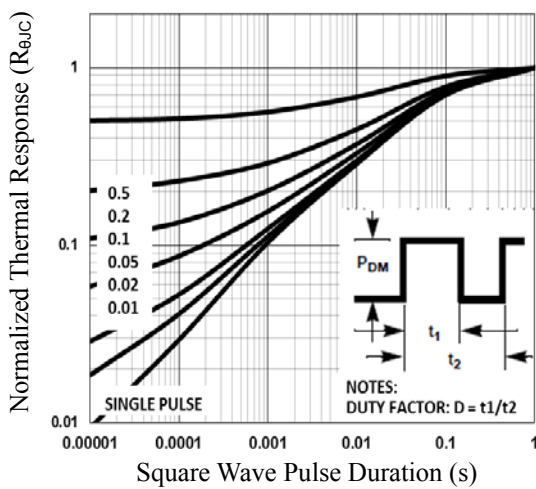


Fig.5 Normalized Transient Impedance

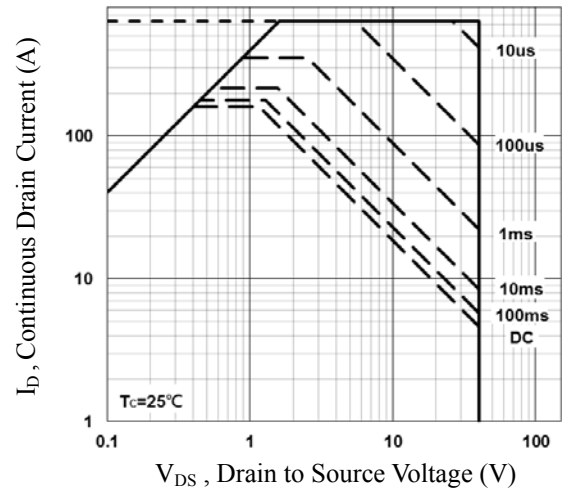


Fig.6 Maximum Safe Operation Area

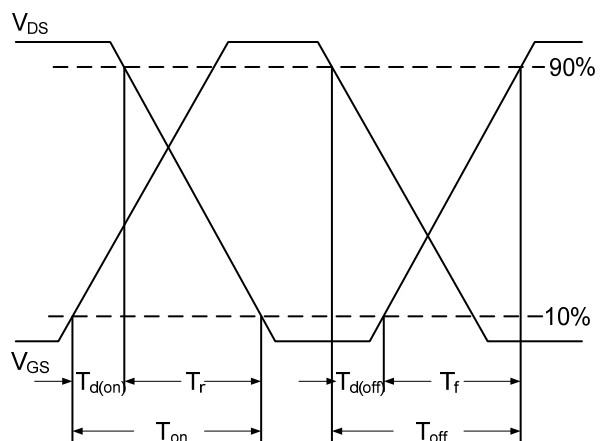


Fig.7 Switching Time Waveform

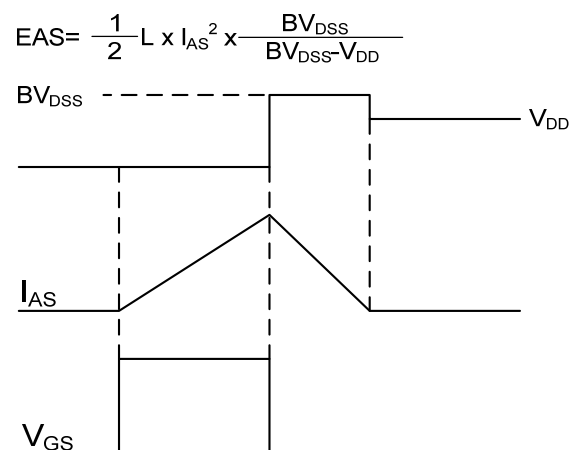
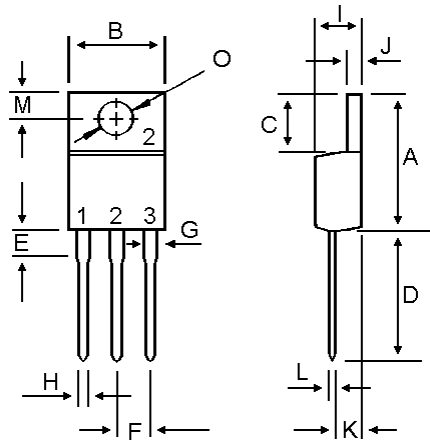


Fig.8 EAS Waveform

$$EAS = \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

TO220 PACKAGE INFORMATION



DIM	MILLIMETERS	
	MIN	MAX
A	14.68	16.00
B	9.78	10.42
C	5.02	6.60
D	13.00	14.62
E	3.10	4.19
F	2.41	2.67
G	1.10	1.67
H	0.69	1.01
I	4.22	4.98
J	1.14	1.40
K	2.20	3.30
L	0.28	0.61
M	2.48	3.00
O	3.50	4.00

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